<u> </u>		
	Application No.	Applicant(s)
	10/616,960	KIM, YONG WAN
Notice of Allowability	Examiner	Art Unit
	Andrew Schechter	2871
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS (herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	plication. If not included will be mailed in due course. THIS
1. This communication is responsive to the filing of 25 April 2005.		
2. The allowed claim(s) is/are 7.9 and 10.		
3. ☑ The drawings filed on <u>11 July 2003</u> are accepted by the Examiner.		
4.		
Attachment(s)  1. Notice of References Cited (PTO-892)  2. Notice of Draftperson's Patent Drawing Review (PTO-948)  3. Information Disclosure Statements (PTO-1449 or PTO/SB/02 Paper No./Mail Date	6. ☐ Interview Summary Paper No./Mail Dat 8), 7. ☐ Examiner's Amendn	e

Art Unit: 2871

## **DETAILED ACTION**

## Allowable Subject Matter

- 1. Claims 7, 9, and 10 are allowed.
- 2. The following is an examiner's statement of reasons for allowance:

In the response of 25 April 2005, the applicants argue that the previous combination of *Shin '449* or *Shin '049* with *Taguchi* would not have been obvious to one of ordinary skill in the art at the time of the invention, since the *Shin* references disclose a pixel electrode separated from the other electrodes by a passivation layer, so the structure is not as susceptible to short circuits as the one in *Taguchi*, nor is the method of *Taguchi* (etching with the gate insulator as an etch-stop) a clearly effective technique. This position finds support in *Taguchi* [col. 23, lines 18-27], which advocates its own technique to correct potential short-circuits of different electrodes on the same layer, but suggests it is unnecessary for electrodes on different layers, where "short circuit defects hardly occur". The examiner finds this argument persuasive and withdraws the previous rejections in view of *Taguchi*.

The prior art does not disclose the device of claim 7, in particular the limitations that there is a passivation layer covering the data wire and the TFT, which is covered by the pixel electrode and exposes the gate insulating layer except portions of the gate insulating layer where the data wire, the TFT, and the pixel electrode are formed. Claim 7 is therefore allowed, as are claims 9 and 10 which depend on it.

Application/Control Number: 10/616,960

Art Unit: 2871

Page 3

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Primary Examiner
Technology Center 2800
5 July 2005